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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/699,903 | 11/03/2003 | Christopher F. Lyons | H0416 / AMDP949US | 4376 |

23623 7590 04/06/2005

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| EXAMINER | |
|---|---|
| MANDALA, VICTOR A | |
| **ART UNIT** | **PAPER NUMBER** |
| 2826 | |

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/699,903 | LYONS ET AL. | |
| | Examiner | Art Unit | |
| | Victor A. Mandala Jr. | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *8-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-7 and 20-22 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,656,763 Oglesby et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

1. Referring to claim 1, a memory device comprising: an array of memory formations, (Col. 14 Lines 39-42), associated with lithographic features of a wafer surface, each memory formation comprising a first electrode, (Figure 2 upper #202), formed from a bit line of the wafer; two second electrodes, (Figure 2 upper#204 & middle #204), positioned sideways, (bottom and upper sides), of the first electrode, (Figure 2 upper #202), on walls of adjacent lithographic features of the wafer surface, to form two memory bits, (Col. 13 Lines 57-65), for one lithographic feature, (Figure 1 #112 and Not specifically shown in Figure 6 #206); and a

selectively conductive media, (Figure 1 #112 and Not specifically shown in Figure 6 #206), placed between the first electrode, (Figure 2 upper #202), and each one of the second electrodes, (Figure 2 upper#204 & middle #204), the first electrode, (Figure 2 upper #202), operable with each of the second electrodes, (Figure 2 upper#204 & middle #204), to selectively activate a memory portion of the selective conductive media, (Figure 1 #112 and Not specifically shown in Figure 6 #206).

2. Referring to claim 2, a memory device, each second electrode, (Figure 2 upper#204 & middle #204), being substantially vertical and stacked laterally next to a side of the first electrode, (Figure 2 upper #202).

3. Referring to claim 3, a memory device, the selectively conductive media, (Figure 1 #112 and Not specifically shown in Figure 6 #206), comprises at least one of a passive material and an organic material, (Col. 3 Line 40-42).

4. Referring to claim 4, a memory device, the organic material is a polymer, (Col. 4 Line 25-26).

5. Referring to claim 5, a memory device, the first electrode, (Figure 2 upper #202), is operative with the second electrode, (Figure 2 upper#204 & middle #204), as to activate a memory portion of the organic material, (Figure 1 #112 and Not specifically shown in Figure 6 #206).

6. Referring to claim 6, a memory device, the selectively conductive material, (Figure 1 #112 and Not specifically shown in Figure 6 #206), is being formed by a depositing system, (Col. 9 Lines 6-7 and Applicant elected the device claims in the election filed on 7/29/04, thus

the method limitation was not elected and the device resulting in no structural difference from the reference).

7. Referring to claim 7, a memory device, the first electrode, (Figure 2 upper #202), formed according to a single or dual damascene process, (Applicant elected the device claims in the election filed on 7/29/04, thus the method limitation was not elected and the device resulting in no structural difference from the reference).

8. Referring to claim 20, a memory device comprising: means for forming two memory elements on sidewalls, (top and bottom sides), of a lithographic feature; and means for sharing an electrode, (Figure 2 upper #202), between the two memory elements, (Figure 1 #112 and Not specifically shown in Figure 6 #206 and Figure 2 upper#204 & middle #204).

9. Referring to claim 21, a memory arrangement comprising: a single electrode, (Figure 2 upper #202), operable with two other electrodes, (Figure 2 upper#204 & middle #204), positioned sideways, (top and bottom sides), thereof, to form two memory elements for one lithographic feature on a wafer surface, each memory element comprising a selective conductive material, (Figure 1 #112 and Not specifically shown in Figure 6 #206), that is sandwiched between the single electrode, (Figure 2 upper #202), and one of the two other electrodes, (Figure 2 upper#204 & middle #204).

10. Referring to claim 22, a memory arrangement, wherein each of the two electrodes, (Figure 2 upper#204 & middle #204), comprising at least one of aluminum, chromium, copper, germanium, gold, magnesium, manganese, indium, iron, nickel, palladium, platinum, silver, titanium, zinc, alloys thereof, indium-tin oxide, polysilicon, doped amorphous silicon and metal silicides, (Col. 3 Lines 50-58).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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3/23/05